

SPECIFICATION

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[METHOD OF HOT SWITCHING DATA TRANSFER RATE ON BUS]

Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 90131022, filed on December 14, 2001.

Background of Invention

[0001] Field of Invention

[0002] The present invention generally relates to data transfer on the bus, and more particularly, to a method of hot switching data transfer rate on the bus.

[0003] Description of Related Art

[0004] In the information explosion era, information processing and information exchange have become more and more important. Since it is so important, how to make the process and information transmission faster is a common objective of present technological development. In the distributed process computer system, between chips that bear different tasks, fast exchange of information is the major factor impacting system performance. Taking the control chips of a computer motherboard as an example, the bus between the north-bridge chip and the south-bridge chip demands a large amount of data transfer. Therefore, its data transfer rate has advanced rapidly. However, while the data transfer rate on the bus has advanced rapidly, power consumption has also increased accordingly. Current computer systems have contradictory needs in data transfer rate and power consumption required to satisfy a sufficient amount of the data transfer rate. Therefore, the data transfer rate on the bus between the control chipsets at present is fixed at a data transfer rate of sufficient amount when the system is up and stable. This data transfer

rate has to take into consideration the maximum transfer demand, but when there is no demand for such a large data transfer rate between the control chipsets, power consumption is still high.

Summary of Invention

[0005] In the view of this, the present invention provides a method of hot switching data transfer rate on the bus, so as to hot switch to higher data transfer rate when the bus between the control chips demands a large amount of data transfer, and hot switch to the lower data transfer rate when the bus between the control chips demands less amount of data transfer, to save power consumption.

[0006] In order to achieve the objective mentioned above and other objectives, the present invention provides a bus wherein the data transfer rate can be hot switched. The bus is used for the command transfer and the data transfer between the first control chip and the second control chip, wherein the data transfer rate can be dynamically switched. During the data transfer rate switching process, the system does not have to reboot. When the first chip receives a transfer rate switching command, the switching method programs the transfer rate register of the first control chip and the second control chip, then determines whether there is no data transaction processed or if the data transaction process is finished. If yes to either, the first control chip subsequently issues a bus release connect command. At this moment, the first control chip and the second control chip enter into the bus release connect state according to the bus release connect command. When either the first control chip or the second control chip issue a bus re-connect command, the first control chip and the second control chip re-connect the bus at the changed data transfer rate according to the content of the data transfer rate register. The bus comprises the data bus, the command signal line and the trigger signal line. The data bus is used to transfer the address and data signal. The command signal line is used to transfer the command signal. The command signal at least comprises the bus release connect command, the bus re-connect command, the data reading command and the data writing command. The trigger signal line is used to synchronously latch the command signal, address and data signal.

[0007] To simplify the bus arbitration mechanism, the command signal line herein should

comprise the unidirectional up command signal line and the unidirectional down command signal line, whereas the trigger signal line should comprise the unidirectional up trigger signal line and the unidirectional down trigger signal line. The bus is suitable for all sorts of control chips that need to exchange information via the bus, such as the north-bridge chip and the south-bridge chip of the computer motherboard. The data transfer rate is switched between, for example, four times the clock frequency of the north-bridge chip and eight times the clock frequency of the north-bridge chip.

[0008] From the description above, by using the method of hot switching the data transfer rate on the bus, the system is no longer limited by a bus data transfer rate that is fixed. The system is able to hot switch to a lower bus data transfer rate when the system does not demand such a large amount of bus data transfer rate, in order to save power consumption. The system applying the present invention is able to hot switch to the higher bus data transfer rate when the system demands a large amount of data transfer, to fulfill the requirement of the data transfer, and then the system applying the present invention is able to hot switch to the lower bus data transfer rate when the system demands a less amount of data transfer, to save power consumption.

Brief Description of Drawings

[0009] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention. In the drawings,

[0010] FIG. 1 schematically shows the bus sketch map of the VLINK BUS of a preferred embodiment according to the present invention;

[0011] FIG. 2 schematically shows the clock sequence diagram when the VLINK BUS of a preferred embodiment according to the present invention is operated at four times the clock frequency;

[0012] FIG. 3 schematically shows the clock sequence diagram when the VLINK BUS of a preferred embodiment according to the present invention is operated at eight times the clock frequency;

[0013] FIG. 4 schematically shows the state diagram of the first control chip and the second control chip of a preferred embodiment according to the present invention;

[0014] FIG. 5 schematically shows the clock sequence diagram when the VLINK BUS of a preferred embodiment according to the present invention enters into the connect state after the system is started;

[0015] FIG. 6 schematically shows the clock sequence diagram when the VLINK BUS of a preferred embodiment according to the present invention enters into the release connect state and re-enters into the connect state;

[0016] FIG. 7 schematically shows the clock sequence diagram when the VLINK BUS of a preferred embodiment according to the present invention enters into the release connect state and re-enters into the connect state at eight times the clock frequency bus data transfer rate; and

[0017] FIG. 8 schematically shows the sketch map of the switching control circuit of the VLINK BUS signal line of a preferred embodiment according to the present invention.

Detailed Description

[0018] The VLINK BUS of a preferred embodiment according to the present invention is exemplified hereafter. FIG. 1 schematically shows the bus sketch map of the VLINK BUS of a preferred embodiment according to the present invention. The VLINK BUS is the bus designed and invented by VIA Technologies, Inc. and is used between control chipsets. As shown in the diagram, the VLINK BUS 100 of the present invention is connected to the first control chip 110 and the second control chip 120, and is used to provide data transfer between these two chips. Herein, the first chip is, for example, the north-bridge chip of the computer motherboard, and the second control chip is, for example, the south-bridge chip of the computer motherboard. As shown in the diagram, the VLINK BUS 100 comprises the data bus (VD[7:0]), the command signal line (UPCMD, DNCMD), the trigger signal line (UPSTB, UPSTB#, DNSTB and DNSTB#), the length/byte enable signal line (VBE), and the common bit check signal line (VPAR). The command signal line comprises the unidirectional up command signal line (UPCMD) and the unidirectional down command signal line (DNCMD). The trigger signal line comprises the unidirectional up trigger signal line (UPSTB, UPSTB#) and the

unidirectional down trigger signal line (DNSTB, DNSTB#). The data bus (VD[7:0]) is used to transfer the address and data signal. The up command signal line (UPCMD) and the down command signal line (DNCMD) are used to transfer the command signal. The command signal at least comprises the bus release connect command, the bus re-connect command, the data reading command, and the data writing command. The up trigger signal line (UPSTB, UPSTB#) and the down trigger signal line (DNSTB, DNSTB#) are used to synchronously latch the command signal, address and data signal transferred by the data bus (VD[7:0]), the up command signal line (UPCMD) and the down command signal line (DNCMD).

[0019] FIG. 2 schematically shows the clock sequence diagram when the VLINK BUS of the present invention is operated at four times the clock frequency. As shown in the diagram, the clock frequency of the first control chip, such as the north-bridge chip of the computer motherboard, is 66 MHz. The clock frequency of the down trigger signal line (DNSTB, DNSTB#) is two times the clock frequency of the first control chip. The down trigger signal line (DNSTB, DNSTB#) is utilized to latch the command signal, address and data signal transferred by the data bus (VD[7:0]) and the down command signal line (DNCMD). It is known that the data transfer rate in the diagram is four times the clock frequency of the north-bridge chip. In the opposite circumstance, the data upload would use a method analogous to this to generate four times the data transfer rate.

[0020] FIG. 3 schematically shows the clock sequence diagram when the VLINK BUS of the present invention is operated at eight times the clock frequency. As shown in the diagram, the clock frequency of the first control chip, such as the north-bridge chip of the computer motherboard, is 66 MHz. The clock frequency of the down trigger signal line (DNSTB, DNSTB#) is four times the clock frequency of the first control chip. The down trigger signal line (DNSTB, DNSTB#) is utilized to latch the command signal, address and data signal transferred by the data bus (VD[7:0]) and the down command signal line (DNCMD). It is known that the data transfer rate in the diagram is eight times the clock frequency of the north-bridge chip. In the opposite circumstance, the data upload would use a method analogous to this to generate eight times the data transfer rate.

connect state and re-enters into the connect state. Referring also to the state diagram of FIG. 4, in FIG. 6, the first control chip 110 issues the bus release connect command via the down command signal line (DNCMD) at 610 as shown in the diagram. The second control chip 120 interprets the bus release connect command of the down command signal line (DNCMD) at 620 as shown in the diagram, so as to enter into the DISCONN1 state accompanied with the first control chip 110 simultaneously. The first control chip 110 and the second control chip 120 enter into the DISCONNECT state simultaneously after one clock period at 630 as shown in the diagram. At this moment, the first control chip 110 and the second control chip 120 deactivate the up trigger signal line (UPSTB, UPSTB#) and the down trigger signal line (DNSTB, DNSTB#) to save the power consumption. In the diagram, when the first control chip 110 and the second control chip 120 are all in the DISCONNECT state, if the second control chip 120 is demanded to transfer data, it enters into the RECONN0 from the state of DISCONNECT. The second control chip 120 then enters into the RECONN1 state at 640 as shown in the diagram, and actively drives a clock period to the up command signal line (UPCMD), indicating the bus re-connect command. The first control chip 110 interprets the bus re-connect command of the up command signal line (UPCMD) at 650 as shown in the diagram. At this moment, the first control chip 110 and the second control chip 120 enter into the RECONN2 state simultaneously, and enter into the CONNECT state simultaneously after two clock periods at 660 as shown in the diagram. At this moment, the up trigger signal line (UPSTB, UPSTB#) and the down trigger signal line (DNSTB, DNSTB#) start to activate to provide the service of fulfilling the data transfer demand.

[0024]

FIG. 7 schematically shows the clock sequence diagram when the VLINK BUS of a preferred embodiment according to the present invention enters into the release connect state and re-enters into the connect state at eight times clock frequency bus data transfer rate. In the diagram, an internal register R8XVK (this is the transfer rate register) and an internal signal MODE8X are provided to the first control chip 110 and the second control chip 120 of the present invention to determine the data transfer rate when the VLINK BUS is re-connected. In the present example, the data transfer rate is four times the bus clock frequency when the R8XVK is in low level, and the data transfer rate is eight times the bus clock frequency when the R8XVK is in high level.

The diagram describes how the bus data transfer rate "hot switches" from four times clock frequency to eight times clock frequency without the RESET to change its data transfer rate. At 710 as shown in the diagram, when the system acknowledges the current bus data transfer rate is obviously insufficient or the higher data transfer rate is demanded, a transfer rate switching command is issued through the application or the device driver to program both of the registers R8XVK in the first control chip 110 and in the second control chip 120 to high level. The first control chip 110 subsequently issues the bus release connect command at 720 as shown in the diagram. Moreover, the first control chip 110 and the second control chip 120 enter into the DISCONNECT state simultaneously at 730 as shown in the diagram. If the first control chip 110 is demanded for bus data transfer, the first control chip 110 drives a clock period to the down command signal line (DNCMD) to indicate the bus re-connect command at 740 as shown in the diagram. The second control chip 120 interprets the bus re-connect command of the down command signal line (DNCMD) at 750 as shown in the diagram. At this moment, the first control chip 110 and the second control chip 120 enter into the RECONN2 state simultaneously. The data latch 810 (FIG. 8) latches the output of the R8XVK to the output port MODE8X at 760 as shown in the diagram. The internal control signal MODE8X is used as the selection input of the multiplexer 820 to selectively output the drive output signal at eight times clock frequency to the bus signal line. At this moment, the up command signal line (UPCMD) and the down command signal line (DNCMD) are also changed from the active low to the active high. Furthermore, after one clock period again at 770 as shown in the diagram, the first control chip 110 and the second control chip 120 enter into the CONNECT state simultaneously. At this moment, the up trigger signal line (UPSTB, UPSTB#) and the down trigger signal line (DNSTB, DNSTB#) start to activate the four times clock frequency. That is, the bus data transfer rate is "hot switched" to the eight times clock frequency at this time.

[0025]

It is known to those skilled in the art that when the system considers that the higher data transfer rate is not demanded, the register R8XVK can be programmed to low level via the application or the device driver to "hot switch" the bus data transfer rate from eight times clock frequency to four times clock frequency without the RESET to change its data transfer rate, so it is only the converse process that is described

above.

[0026] The descriptions mentioned above provide a method of hot switching data transfer rate on the bus to dynamically switch the data transfer rate in between the first control chip and the second control chip, and in the data transfer rate switching process, the RESET is not needed. The method comprises the steps of: at first, the first control chip and the second control chip receive a transfer rate switching command; then, when there is no data transaction processed or the data transaction processed is finished, the first control chip issues a bus release connect command; afterwards, the first control chip and the second control chip enter into the bus release connect state according to the bus release connect command; when the data transfer is demanded, the first control chip and the second control chip issue a bus re-connect command; at this moment, the first control chip and the second control chip re-connect to the changed bus data transfer rate according to the transfer rate switching command.

[0027] Therefore, it is known that by using the method of the hot switching data transfer rate on the bus, the system is no longer limited by a bus data transfer rate that is fixed to a certain amount. The system is able to hot switch to the lower bus data transfer rate when the system does not demand such a large amount of the bus data transfer rate to save the power consumption. That is, the system applying the present invention is able to hot switch to the higher bus data transfer rate when the system demands a large amount of data transfer to fulfill the requirement of the data transfer. Contrarily, the system applying the present invention is able to hot switch to the lower bus data transfer rate when the system demands a less amount of data transfer to save the power consumption.

[0028] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.